and activation of dopants the edges of doped regions generally may not be straight lines and the corners may not be precise angles.

In addition, the description may illustrate a cellular design (where the body regions are a plurality of cellular regions) instead of a single body design (where the body region is comprised of a single region formed in an elongated pattern, typically in a serpentine pattern). However, it is intended that the description is applicable to both a cellular implementation and a single base implementation.

DETAILED DESCRIPTION OF THE DRAWINGS

In general, the present embodiments relate to a structure and a method of forming the structure for high electron mobility ("HEM") devices. The HEM devices include a base semiconductor substrate and a heterostructure associated with the base substrate. In some embodiments, the heterostructure is a III-nitride series material such as gallium nitride (GaN), aluminum gallium nitride (AlGaN), indium nitride (InN), aluminum nitride (AlN), indium gallium nitride (InGaN), indium aluminum gallium nitride (InAlGaN), or similar materials as known to those of skill in the art. The base semiconductor substrate provides a first current carrying electrode for the HEM device. In some embodiments, a gate structure is provided adjacent a major surface of the heterostructure and a second current carrying electrode is on the major surface but spaced apart from the gate structure.

In some embodiments, the heterostructure includes a GaN channel layer and an AlGaN barrier layer. In some embodiments, at least one internal connector structure extends through the heterostructure to the base semiconductor substrate to provide a low resistance electrical current path from the base substrate to regions of the device proximate to the barrier layer. In some embodiments, the internal connector structure can include first and second conductors. In some embodiments, the internal connector structure includes at least one trench formed in the heterostructure and a portion of the base semiconductor substrate. In some embodiments, the trench is lined with an insulating material and further lined or filled with a conductive material adjacent the insulating material. In other embodiments, the HEM device is integrated with a MOSFET device in a monolithic single-chip configuration.

Attributes of the method and structure described hereinafter provide for the routing of source and gate conductive lines on the top surface of a die with the drain conductive layer on the back surface of the die. In some embodiments, both the source and gate terminals are biased at low voltage, which puts a lower stress on inter-metal dielectric structures. This lower stress reduces electro-migration issues. The structure also provides for semiconductor chip area savings of at least 30% because bonding to the source and gate terminals can be done over the active area of the device. Additionally, the configuration facilitates the assembly of the HEM devices with other devices such as silicon MOSFET devices, which reduces parasitic inductances and resistances compared to related devices.

FIG. **1** illustrates an enlarged cross-sectional view of an embodiment of a semiconductor device **10** configured as a III-nitride depletion mode high electron mobility transistor ("HEMT"). Transistor **10** includes a base substrate, base semiconductor substrate, a region of semiconductor material, semiconductor region, or semiconductor substrate **11**. In several embodiments, substrate **11** is a silicon substrate having a (111) orientation and is doped with an n-type dopant such as phosphorous, arsenic or antimony. In other embodiments, substrate **11** can have other orientations. In other embodiments, substrate **11** can be silicon-carbide or other semiconductor materials that can be doped to form a current carrying electrode. In several embodiments, substrate **11** has a low resistivity (that is, has a high dopant concentration) with a resistivity in a typical range from about 0.001 to about 0.01 ohm-cm. In the present embodiment, transistor **10** also includes an optional field extension layer **12**, which can be a lower doped n-type silicon epitaxial layer. In other embodiments, field extension layer **12** can be lower doped p-type conductivity. The thickness of field extension layer **12** depends on the required blocking voltage of transistor **10** and a typical thickness is in a range from 2 microns to about 20 microns.

Transistor **10** also includes a heterostructure or epitaxial structure **13**, which can be formed on substrate **11** or field extension layer **12** if field extension layer **12** is included. In several embodiments, heterostructure **13** includes a plurality of layers including, for example, a nucleation or buffer layer **16**, one or more buffer or transition layers **17**, a channel layer **19**, and a barrier layer **21**. In some embodiments, buffer layer **16** can be, for example, an MN layer situated over field extension layer **12**. One or more transition layers **17**, which can be optional in some embodiments, can be formed situated over buffer layer **16**. In some embodiments, transition layers **17** can be, for example, AlGaN with varying amounts of aluminum concentration. For example, the aluminum concentration can be higher in the transition layers **17** closer to buffer layer **16** and lower closer to channel layer **19**.

Channel layer **19** can be formed situated over buffer layer **16** or optional transition layers **17**. In several embodiments, channel layer **19** can be, for example, a GaN layer. In some embodiments, barrier layer **21** can be AlGaN and formed over channel layer **19**. At the interface of the AlGaN layer **21** and the GaN channel **19** a two-dimensional electron gas (2DEG) layer or region **22** is created, as known to those of ordinary skill in the art.

In some embodiments, transistor **10** further includes a gate dielectric layer or region **26** situated over a portion of barrier layer **21** as illustrated in FIG. **1**. In other embodiments, transistor **10** can be configured with a Schottky gate. In some embodiments, gate dielectric region **26** can be silicon nitride, aluminum nitride, aluminum oxide, silicon dioxide or combinations thereof, hafnium oxide, or other materials as known to those of ordinary skill in the art. A control or gate electrode **27** is situated over gate dielectric region **26**, and can be, for example, aluminum with a titanium and/or titanium-nitride barrier or other conductive materials as known to those of ordinary skill in the art. As illustrated in FIG. **1**, transistor **10** can also include an insulation or insulative layer or layers **31** situated over portions of major surface **28** of heterostructure **13**, which can be, for example, silicon nitride, aluminum nitride, combinations thereof, or other insulative materials as known to those of ordinary skill in the art. In some embodiments, insulation layer **31** can be silicon nitride formed using plasma-enhanced chemical vapor deposition techniques ("PECVD"), low pressure chemical vapor deposition ("LPCVD"), metal organic chemical vapor deposition ("MOCVD"), or atomic layer deposition ("ALD"), and can have a thickness in some embodiments from about 0.1 microns to about 0.2 microns. In some embodiments, the silicon nitride forms a field plate that reduces the effect of the high electric fields that can be formed between the drain and gate regions.